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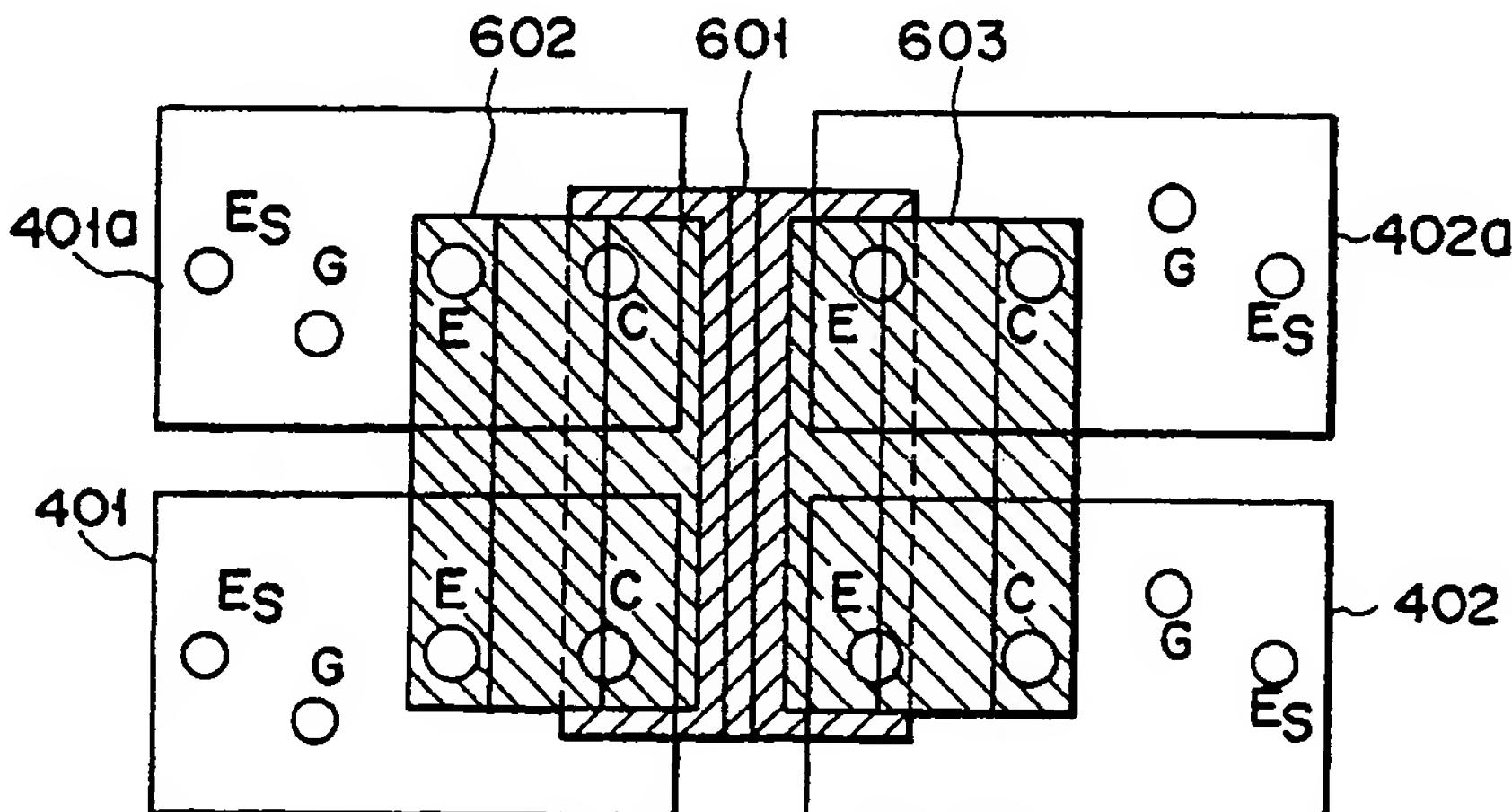
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㉒ Module-type semiconductor device of high power capacity.

㉓ One of a pair of the module type semiconductor devices (401, 401a), signal input terminals (Es, G) are located on the other side of current output terminals (E) with respect to current input terminals (C), and that, in the other of a pair of the module type semiconductor devices (402, 402a), signal input terminals are mounted on the other side of current input terminals with respect to current output terminals. Distance of connections between element in

the case of bridge connections may be shortened to the minimum. Since the signal input terminals (Es, G) may be located outside the bus bars (601, 602, 603) openings need not be formed in the bus bar. Space or the bus bar's surface area thus may be effectively used, with the result that a decrease in commutating inductance is achieved.



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F I G. 6A

This invention relates to the arrangement of external terminals of a high power semiconductor device, such as an IGBT (insulated gate bipolar transistor) or a MOS FET, capable of high speed switching with high power and, more particularly, to the arrangement of module type semiconductor devices of high power capacity.

IGBTs, representative of high speed and high power switching elements, have heretofore been formed of module casings having a structure shown in Figs. 1A and 1B. Fig. 1C shows an equivalent circuit of the IGBT.

In Figs. 1A and 1B, a collector C and an emitter E forming main current terminals, and a gate G and an emitter Es forming input terminals for drive signals are used as corresponding, respectively, to a collector C and an emitter E forming main current terminals in a bipolar transistor 101 shown in Fig. 1C, and a base B and an emitter Es forming signal input terminals of same. Between the collector and the emitter is interposed a portion that functions similar to a diode, and hence a diode 102 is incorporated therebetween.

Within the module casing shown in Figs. 1A and 1B are incorporated a plurality of, usually four, IGBT chips for being driven in parallel, thereby completing a high current semiconductor switching module.

The foregoing arrangement is disclosed in a publication entitled "1000V 300A Bipolar-Mode MOS FET (IGBT) Module", 1988 Proc. of ISPSD, pp 80-85, M. Hidesima, et al.

In some applications, a plurality of module type semiconductor devices of high power capacity of the arrangement shown in Figs. 1A and 1B are connected in parallel to each other to obtain a circuit, such as an inverter, of further increased power capacity. In this case, it may be proposed to provide an ultra high power semiconductor device without connecting a plurality of modules but sealing several of modules in a single module casing. This, however, is not preferred on the following grounds.

First, the range of general applications of the module type semiconductor device becomes limited. Second, the number of parallel connections of IGBT chips within the module type semiconductor device become too excessive that the productivity of the device is decreased. Third, with an increase in a value of the current managed by a single module, wiring requirements within the device increase. Accordingly, use of module type semiconductor devices in parallel connections each having IGBT chips sealed within the casing in a convenient number of four is believed to be economical in high power capacity applications.

Fig. 2 is a circuit diagram showing the arrangement of a bridge-type chopper circuit using the

module type semiconductor device of high capacity. Equivalent circuits Q1 to Q4 representing the IGBTs and each formed of a module type semiconductor device fabricated with a conventional module package shown in Figs. 1A and 1B are connected two by two in parallel to obtain a high capacity. A half bridge structure showing the interconnections of the equivalent circuits Q1 and Q2 in Fig. 2 is illustrated in Fig. 3A. As shown, the module type semiconductor devices 301 and 302 are connected in parallel to form the equivalent circuit Q2, and the module type semiconductor devices 303 and 304 having equivalent properties as the devices 301 and 302 are connected in parallel to form the equivalent circuit Q1. A bus bar 305 connects main current terminals of the respective emitters of the module type semiconductor devices 301 and 302, and a bus bar 306 connects main current terminals of the respective collectors of the module type semiconductor devices 303 and 304. Further, a bus bar 307 makes interconnections between the collector main current terminals of the module type semiconductor devices 301 and 302, between the emitter main current terminals of the module type semiconductor devices 303 and 304, and between the module type semiconductor devices 301 and 302, and 303 and 304. The structure as viewed from an arrow 310 in Fig. 3A is shown in Fig. 3B.

As shown in Figs. 3A and 3B, it is necessary to form openings 307a and 307b in the bus bar 307 at locations above signal input terminals Es and G of the module type semiconductor devices 303 and 304 to enable wiring connections to the signal terminals.

It has been found that, when the module type semiconductor devices fabricated with the module casing as shown in Figs. 1A and 1B are subjected to bus bar wiring as shown in Figs. 3A and 3B, a problem occurs that as the proposed current capacity of the module type semiconductor device increases and the proposed speed of switching operation increases, an inductance component of commutating circuits which increases surge voltage becomes not negligible, requiring setting a large margin for the voltage withstandability of the circuit elements.

Moving to Fig. 2, the mechanism of commutating operation and the generation of surge voltage will be explained. The circuit shown is a so-called bridge circuit in which the IGBTs Q1 and Q2 are connected in series between a bus 202 and a bus 203 leading from a DC power supply 201, the IGBTs Q3 and Q4 are similarly connected in series therebetween, and an electric reactor 204 and a resistor 205 are connected between connecting points midway between the respective series connection lines.

Assume now that the IGBTs Q1 and Q4 are on

and current is flowing through the circuit shown by arrows in solid lines. If the IGBT Q1 is turned off, a load current commutes through the circuit shown by an arrow in a dotted line. At this time, inductance L of the circuit and the rate of change of current  $di/dt$  generate a counter electromotive force of  $-L(di/dt)$  as surge voltage, which is impressed across the IGBT Q1 which has been turned off.

The inductance L here is affected by an inductance component of the bus 202 between nodes a and b, an inductance component of the bus 203 between nodes h and i, inductance components of the wiring between nodes b and c and between d and e, and by inductance components of the wiring between nodes e and f and between g and h.

If, for example, the inductance L is  $0.2 \mu\text{H}$  and an IGBT with a current of 400A is turned off at time intervals of  $0.3 \mu\text{s}$ , the following equation holds.

$$V = L(di/dt) \\ = 0.2 \times (10^{-6} \times 400) / (0.3 \times 10^{-6}) = 270 \text{ V} \quad (1)$$

Equation (1) suggests the production of a surge voltage of approximately 270V. To use an IGBT element at 500 V in the circuit arrangement shown in Fig. 2, it is necessary to use the voltage of the power supply at 230 V or below, so that use of IGBTs becomes limitative.

Where a module type semiconductor device of a package of the structure shown in Figs. 1A and 1B is used, what has been done in an attempt to decrease inductance components as far as possible is to permit the collector C of the module forming Q1 and the emitter E of the module forming Q2 to be connected by a copper plate and to punch out the copper plate at portions of the terminals G and Es. This has resulted in lengthy wiring and limited surface area of the copper plate and hence in an increase in commutating inductance. With increasing demand on still higher speed operation of module type semiconductor devices, a decrease in the commutating inductance has been sought.

According an object of the invention is to provide a module type semiconductor device having a shortened length of interconnection wiring, a large surface area of the wiring and a bridge connection structure capable of canceling magnetic flux to be generated by commutating current, with a view to minimizing commutating inductance.

According to a first embodiment of the invention, a pair of high power module type semiconductor devices are provided which comprise first and second casings of a substantially equivalent type; power semiconductor devices of substantially equivalent electrical properties sealed respectively within the first and second casings; and external terminals formed of current input terminals, current output terminals and signal input terminals of the power semiconductor devices, which are taken ex-

ternally of the first and second casings from top thereof; the external terminals taken externally of the first casing having a terminal arrangement in which the signal input terminals are located on an opposite side of the current output terminal with respect to the current input terminal, and the external terminals taken externally of the second casing having a terminal arrangement in which the signal input terminals are located on an opposite side of the current input terminal with respect to the current output terminal.

Where the first casing and the second casing are bridge connected by a bus bar with the above mentioned arrangement, distances of connections between elements may be shortened to a minimum. Since signal input terminals may be located outside the bus bar, openings for exposure of signal input terminals need not be formed in the bus bar structure, so that the overall structure is simplified to make effective use of a surface area of the bus bar, with the result that a decrease in commutating inductance is achieved.

A second embodiment of the invention provides a module type semiconductor device of high power capacity which comprises a having a projecting central portion whose top is plane casing sealing therein at least one pair of semiconductor chips for forming a power semiconductor device and having two different planes; a current input terminal and a current output terminal taken externally of the casing at the projecting central portion thereof and from one of the planes higher than the other plane of the power semiconductor device; and two pairs of equivalent signal input terminals located on a lower plane positioned on both sides of the central higher plane and connected in common with the casing.

Similar effects as in the first embodiment may be obtained by fabricating a structure using the above module type semiconductor device in a pair. The device according to this embodiment is suitable for mass production since there is only a single layout for terminals that are taken out of the casing.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1A is a plan view illustrating the outer appearance of a conventional module casing for a module type semiconductor device (IGBT);

Fig. 1B is a side view of the structure shown in Fig. 1A;

Fig. 1C is an equivalent circuit of the IGBT;

Fig. 2 is a circuit diagram showing the structure of an application circuit to which this invention relates;

Fig. 3A is a plan view showing the form of

mounting of mutually connected module type semiconductor devices (IGBTs) of a known type; Fig. 3B is an outside view of the structure shown in Fig. 3A as viewed from the side;

Fig. 4A is a plan view showing the appearance of a module package of one of a pair of module type semiconductor devices according to the first embodiment of the invention;

Fig. 4B is a view similar to Fig. 4A showing the appearance of a module casing of the other of the pair of module type semiconductor devices according to the first embodiment of the invention;

Fig. 4C is a side view of the structure shown in Fig. 4A;

Fig. 4D is a side view of the structure shown in Fig. 4B;

Fig. 5 is a perspective view showing the inside structure of the module type semiconductor devices according to this invention;

Fig. 6A is a plan view showing the form of mounting of mutually connected module type semiconductor devices (IGBTs) according to the first embodiment of the invention;

Fig. 6B is a view showing the appearance of the structure of Fig. 6A as viewed from the side;

Fig. 7A is a plan illustrating the appearance of a module package of module type semiconductor devices according to the second embodiment of the invention;

Fig. 7B is a side view of the structure shown in Fig. 7A; and

Fig. 8 is a view showing the form of mounting of mutually connected module type semiconductor devices (IGBTs) as viewed from the side, in accordance with the second embodiment of the invention.

The embodiments of the invention will be described with reference to the accompanying drawings. Figs. 4A, 4B, 4C and 4D show the appearance of module type semiconductor devices according to the first embodiment. It is a feature that a pair of module type semiconductor devices 401 and 402 form a set.

In particular, the arrangement of terminals of the module type semiconductor device 401 forming an IGBT is in the order of signal input terminals E<sub>s</sub> and G, and an emitter E and a collector C forming main current external terminals. In contrast, in the module type semiconductor device 402, the order of the emitter E and the collector C is opposite, and they are in the order of signal input terminals E<sub>s</sub> and G, the collector C and the emitter E forming the main current external terminals.

A pair of the module type semiconductor devices 401 and 402 are structured with equivalent electrical properties, and their inside structures are as shown in Fig. 5. In the figure, two insulating

substrates 502a and 502b of an identical nature are soldered on a heat radiation substrate 501. On the insulating substrate 502a are fixed a metal plate 503a and relaying metal plates 504a and 505a on both sides of the metal plate 503a. Likewise, on the insulating substrate 502b are fixed a metal plate 503b and relaying metal plates 504b and 505b on both sides of the metal plate 503b. Identical semiconductor chips 506 are mounted two by two on each of the metal plates 503a and 503b.

Wiring of electrodes on the semiconductor chips 506, here an emitter and a gate, is effected such that the emitter is connected to the metal plates 504a and 504b by metal wiring lines 507, and the gate is connected to the metal plates 505a and 505b by metal wiring lines 507. A power semiconductor device 508 is thus structured.

While not illustrated, a metal lead acting as an external terminal common to the two relaying metal plates 504a and 504b is soldered to form a main current external terminal of the emitter. Further, a metal lead acting as an external terminal common to the two relaying metal plates 503a and 503b is soldered to constitute a signal input external terminal of the gate. A metal lead acting as an external terminal common to the two relaying metal plates 504a and 504b is soldered to form a signal input external terminal of the emitter.

These external terminals are fabricated to have a terminal structure shown in the module type semiconductor device 401 or 402 of Figs. 4A and 4B. For example, in forming main current external terminals of the emitter and the collector, two kinds of external terminal metal lead may be used so that the positioning of the main current terminals of the collectors and the emitters which are externally taken out of the semiconductor devices is mutually opposite.

Instead of connecting the relaying metal plates 504a and 505a, or 504b and 505b to the external terminals, the plates themselves may be externally taken out as external terminals.

As a result of this, a pair of module type semiconductor devices 401 and 402 having the terminal arrangement as shown in Figs. 4A, 4B, 4C and 4D are constituted. A resin casing 403 is bonded on the heat radiation substrate 501 shown in Fig. 5. The resin casing 403 is resin sealed to protect the semiconductor chips and the other component elements shown in Fig. 5.

A pair of the module type semiconductor devices 401 and 402 may form a half bridge circuit as shown in Figs. 6A and 6B by employing another set of a pair of the devices designated by reference numerals 401a and 402a. Wiring interconnections of elements as those of Q1 and Q2 in the circuit arrangement of Fig. 2 are as follows.

The collector terminals C of the semiconductor

device 401 and 401a and the emitter terminals E of the devices 402 and 402a are interconnected by a bus bar 601 and externally taken out as an output electrode. A positive electrode of the DC power supply (bus 202 side in Fig. 2) is connected to a bus bar 602, and a negative electrode (bus 203 side in Fig. 2) to a bus bar 603. The bus bars 602 and 603 are disposed in as parallel as possible to and in as close as possible proximity to the bus bar 601. The bus bar 602 is connected to the emitter terminals E of the semiconductor devices 401 and 401a, and the bus bar 603 is connected to the collector terminals C of the semiconductor devices 402 and 402a.

As has been described, the module type semiconductor devices in pairs shown in Figs. 4A to 4D and 6A and 6B in accordance with the first embodiment are featured by the arrangement that, in one of a pair of the module type semiconductor devices, signal input terminals (corresponding to Es and G) are located on the other side of current output terminals (corresponding to the emitter terminals E) with respect to current input terminals (corresponding to the collector terminals C), and that, in the other of a pair of the module type semiconductor devices, signal input terminals are mounted on the other side of current input terminals with respect to current output terminals. The above construction produces the following functions and meritorious effects.

1. Pairs of module type semiconductor devices are easily fabricated using all of the components in common, except for the preparation of two kinds of external terminal metal leads for connection with the relaying metal plates. There are almost no differences in electrical properties between the pair of the semiconductor devices.
2. Distances of connections between elements in the case of bridge connections may be shortened to the minimum. Since the signal input terminals may be located outside the bus bars 601, 602 and 603, openings such as those 306a and 306b formed in the bus bar 306 in Fig. 3A need not be formed. Space or the surface area of the bus bar thus may be effectively used.
3. The bus bars 602 and 603 leading to the electrodes on the side of the bus 202 and on the side of the bus 203 in the bridge circuit shown in Fig. 2 are capable of being projected upright in parallel to the bus bar 601 functioning as a connector electrode between elements, so that magnetic fluxes to be generated by the bus bars at turn-on times may be cancelled. The amount of commuting inductance may thus be kept minimum.

Item 3 above will be expanded with reference to Fig. 2. When current commutes as shown by an arrow in a dotted line upon turn-off of the IGBT

Q1, which occurs subsequent to a stage in which the IGBTs Q1 and Q4 are turned on to allow current to flow as shown by arrows in solid lines, magnetic fluxes between the conductive busses between a and b and between h and i are canceled and inductance is minimum if the busses are wired in close proximity to each other. On the other hand, if the nodes between b-c and d-e of the IGBT Q1 are brought in close proximity to each other and wiring is effected to permit the direction of current flow is to be inverted, inductance therebetween is also minimum. Further, bringing the nodes between e-f and g-h in the IGBT Q2 in close proximity to each other to cancel magnetic fluxes, inductance therebetween is also brought to a minimum.

With the above arrangement, a bridge circuit, such as one shown in Fig. 2, may have bus bar wiring as shown in Figs. 6A and 6B, even if Q1 and Q4 are arranged by parallel connecting a plurality of module type semiconductor devices, regardless of the number of parallel interconnections. The inductance of the commuting circuit is thus made minimum. As a result, surge voltage at the time of commutation, to be generated upon turn-on and off of the IGBTs may be greatly decreased. The second embodiment illustrated in Figs. 7A and 7B provides a novel package configuration for achieving the structure of a pair of the module type semiconductor devices shown in Figs. 4A to 4D by a single module type semiconductor device. A half bridge circuit in which the module type semiconductor devices according to the second embodiment are connected in parallel is shown in Fig. 8.

In Figs. 7A and 7B, on both sides of the collector C and the emitter E which are the main current terminals is mounted a pair of signal input terminals Es and G, which are interconnected to each other within the module. The input of signals can thus be effected using only one of the pair of the signal input terminals. A plane on which the signal input terminals Es and G are located is set lower than a plane on which the main current terminals E and C are positioned.

Two of the module-type semiconductor device 701, denoted by reference numerals 701-1 and 701-2, may be wired by bus bars 801, 802 and 803 as shown in Fig. 8. Terminals Es and G of the respective semiconductor devices 701-1 and 701-2 are used as signal input terminals and terminals Es' and G' located inwardly of the devices are not used, so that the inductance of the commuting circuit can be minimized similarly as in the first embodiment shown in Figs. 6A and 6B.

While the length of the bus bar 801 in Fig. 8 is slightly longer than the bus bar 601 in Fig. 6B, the increase of inductance is negligibly small inasmuch as the bus bar 801 may be positioned in parallel to and in close proximity to the bus bars 802 and 803.

In Figs. 7A and 7B, the non used signal input terminals Es and G are formed on a plane lower than that of the main current terminals E and C, so that the presence of the non used signal input terminals G and Es is not at all a bar to linearly connecting the collector C of the semiconductor device 701 and the emitter E of the semiconductor device 701a by the bus bar 801. In comparison with the first embodiment, this arrangement has an advantage in that the terminals that are taken out externally of the casing are in a single pattern or arrangement, so that the structure is suited for mass production.

In the foregoing embodiments, the signal input terminals Es and G have been described as an example of screw terminals, they may of course be in fastening terminals configuration, etc. Further, the IGBTs have been described as an example of the module type semiconductor device according to this invention, the invention is applicable also to usual MOS FETs, bipolar transistors, etc. Needless to say, the effects of the invention are most conspicuously displayed in IGBT speed switching function.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

### Claims

1. A module type semiconductor device of a high power capacity comprising:  
first and second casings (401, 402) of a substantially equivalent type;  
power semiconductor devices (508) of substantially equivalent electrical properties sealed respectively within said first and second casings (401, 402); and  
external terminals formed of current input terminals (C), current output terminals (E) and signal input terminals (G, Es) of said power semiconductor devices, which are taken externally of said first and second casings (401, 402) from top thereof;  
the external terminals taken externally of said first casing having a terminal arrangement in which the signal input terminals (G, Es) are located on an opposite side of the current output terminal (E) with respect to said current input terminal (C), and the external terminals taken externally of said second casing having a terminal arrangement in which the signal input terminals (G, Es) are located on an opposite side of the current input terminal (C) with respect to the current output terminal (E).
2. The module type semiconductor device according to claim 1, characterized in that said first and second casings (401, 402) are formed respectively of a resin.
3. The module type semiconductor device according to claim 1, characterized in that said power

- 5 semiconductor devices (508) sealed within said first and second casings (401, 402) respectively with substantially equivalent electrical properties comprise pairs of semiconductor chips (506) having substantially equivalent electrical properties.
- 10 4. The module type semiconductor device according to claim 3, characterized in that said semiconductor chips (506) have a layout for said power semiconductor devices, which is common both within said first and second casings (401, 402).
- 15 5. The module type semiconductor device according to claim 1, characterized in that said external terminals (E, C, G, Es) are screw terminals.
- 20 6. The module type semiconductor device according to claim 1, characterized in that said signal input terminals (G, Es) are fastening configuration terminals.
- 25 7. The module type semiconductor device according to claim 1, characterized in that said first and second casings (401, 401a, 402, 402a) are formed on a plane in a pair such that the current input terminal (C) of the power semiconductor device (508), which is taken externally of said first casing (401, 401a) and the current output terminal (E) of the power semiconductor device (508), which is taken out of said second casing (402, 402a) are in close proximity to and oppose each other, and which further comprises:  
30 a first bus bar (601) electrically interconnecting said opposing current input terminal (C) and current output terminal (E) at a least distance and which is taken out externally upwardly as an electrode;
- 35 35 a second bus bar (602) located in as parallel as possible to and in as close as possible proximity to said first bus bar (601) on one side thereof and electrically connected to the current output terminal (E) of the power semiconductor device (508), which is taken externally of said first casing (401, 401a); and
- 40 40 a third bus bar (603) located in as parallel as possible to and in as close as possible proximity to said first bus bar (601) on the other side thereof and electrically connected to the current input terminal (C) of the power semiconductor device (508), which is taken externally of said second casing (402, 402a).
- 45 45 8. A module type semiconductor device of a high power capacity comprising:  
50 a casing having a projecting central portion whose top is plane (701) sealing therein at least one pair of semiconductor chips (506) for forming a power semiconductor device (508) and having two different planes;  
55 a current input terminal (C) and a current output terminal (E) taken externally of the casing (701) at the projecting central portion thereof and on one of the planes higher than the other plane of the power

semiconductor device (701); and  
two pairs of equivalent signal input terminals (G, Es) located on a lower plane positioned on both sides of the projecting central portion and connected in common with the casing.

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9. The module type semiconductor device according to claim 8, characterized in that said casing (701) is formed of a resin.

10. The module type semiconductor device according to claim 8, characterized in that said semiconductor chips (506) forming the power semiconductor device (508) sealed within said casing are two or more and having substantially equivalent electrical properties.

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11. The module type semiconductor device according to claim 8, characterized in that the current input terminal (C), the current output terminal (E) and the two pairs of signal input terminals (G, Es) are, respectively, screw terminals.

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12. The module type semiconductor device according to claim 8, characterized in that the current input terminal (C), the current output terminal (E) and the two pairs of signal input terminals (G, Es) are, respectively, fastening configuration terminals.

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13. The module type semiconductor device according to claim 8, characterized in that each of the pairs of signal input terminals (G, Es) of said casings (701-1, 701-2) opposes the other pair in close proximity to each other, and which further comprises:

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a first bus bar (801) electrically interconnecting said opposing current input terminal (C) and current output terminal (E) at a least distance and which is taken out externally upwardly as an electrode;

30

a second bus bar (802) located in as parallel as possible to and in as close as possible proximity to said first bus bar (801) on one side thereof and electrically connected to the current output terminal (E) of the power semiconductor device, which is taken externally of one (701-1) of said casings; and a third bus bar (803) located in as parallel as possible to and in as close as possible proximity to said first bus bar (801) on the other side thereof and electrically connected to the current input terminal (C) of the power semiconductor device, which is taken externally of the other (701-2) of said casings.

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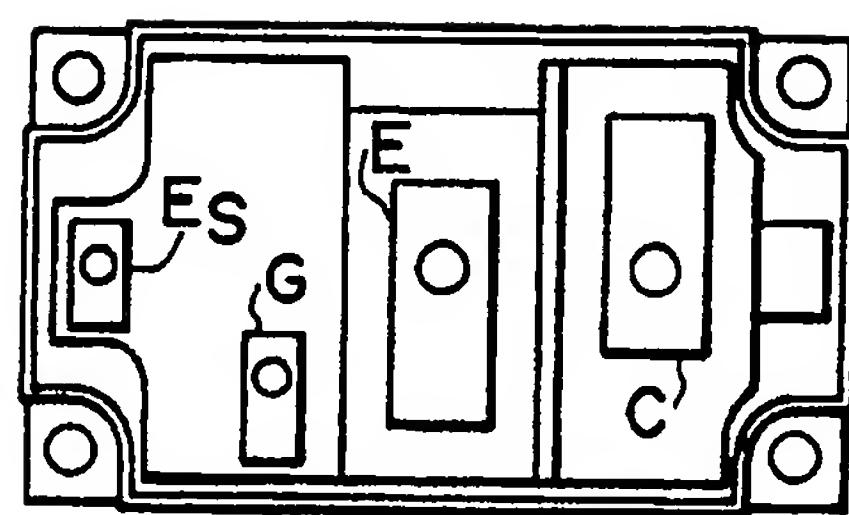


FIG. 1A

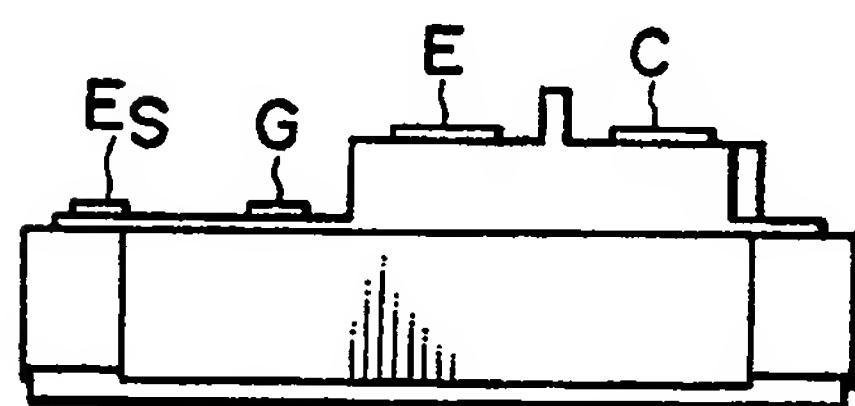


FIG. 1B

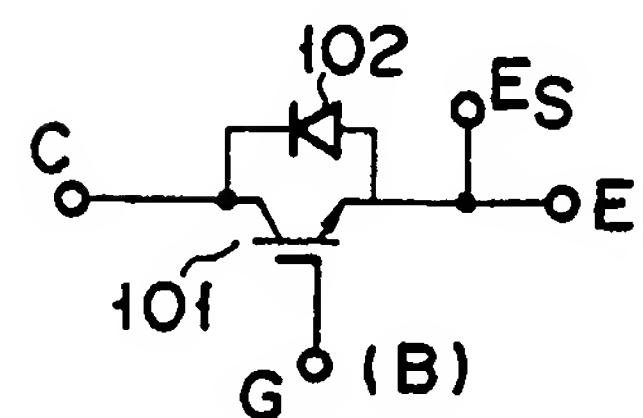


FIG. 1C

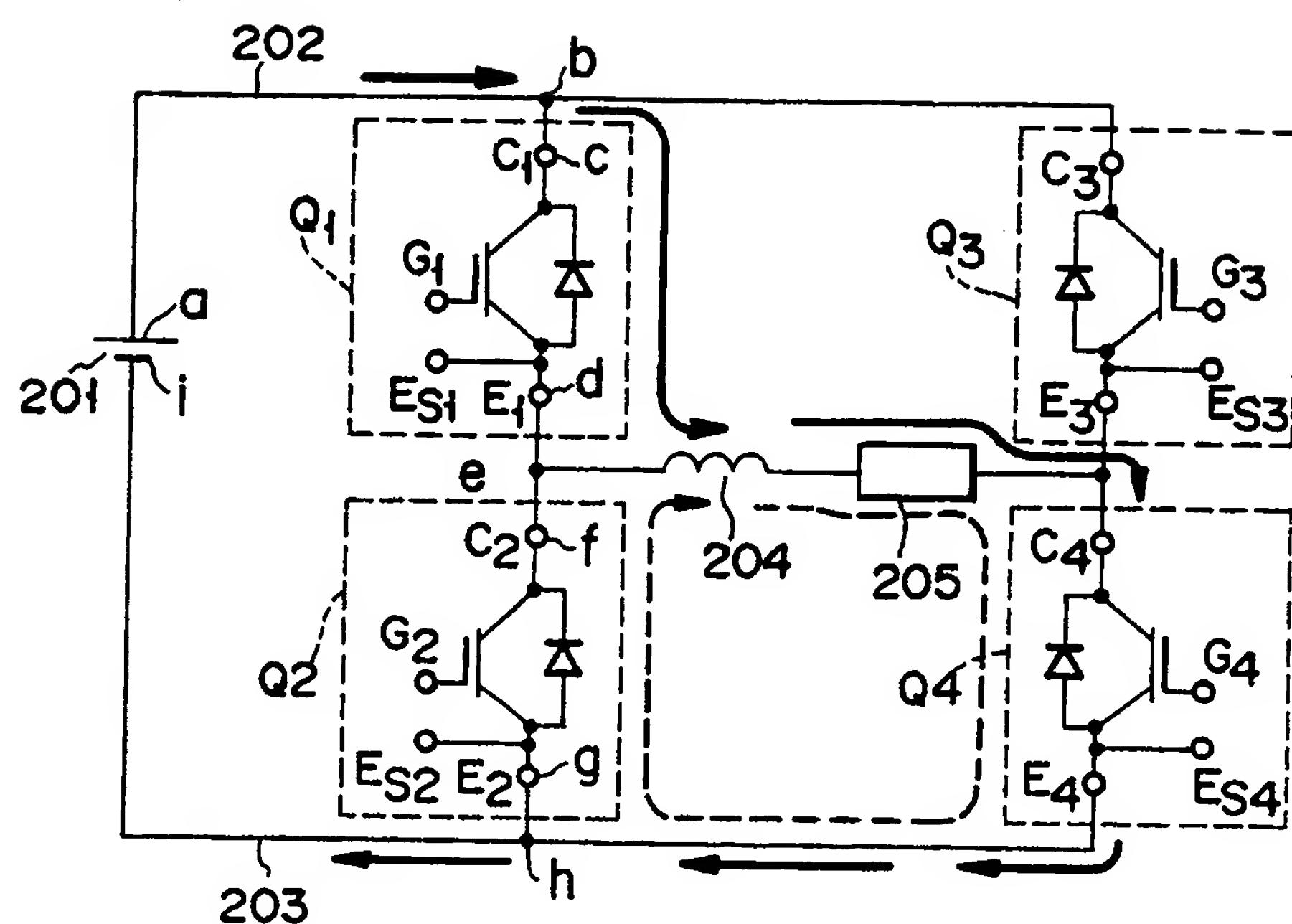
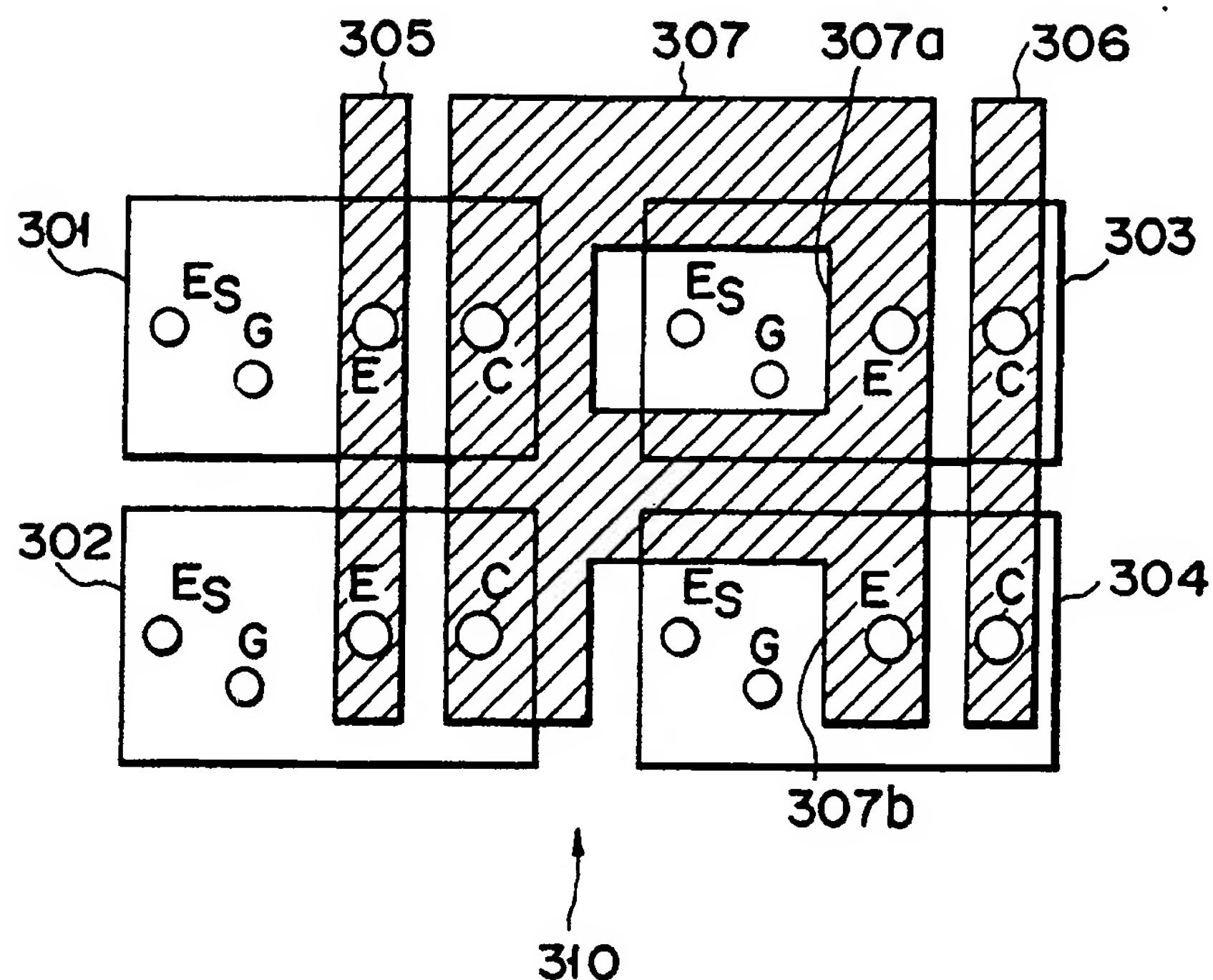
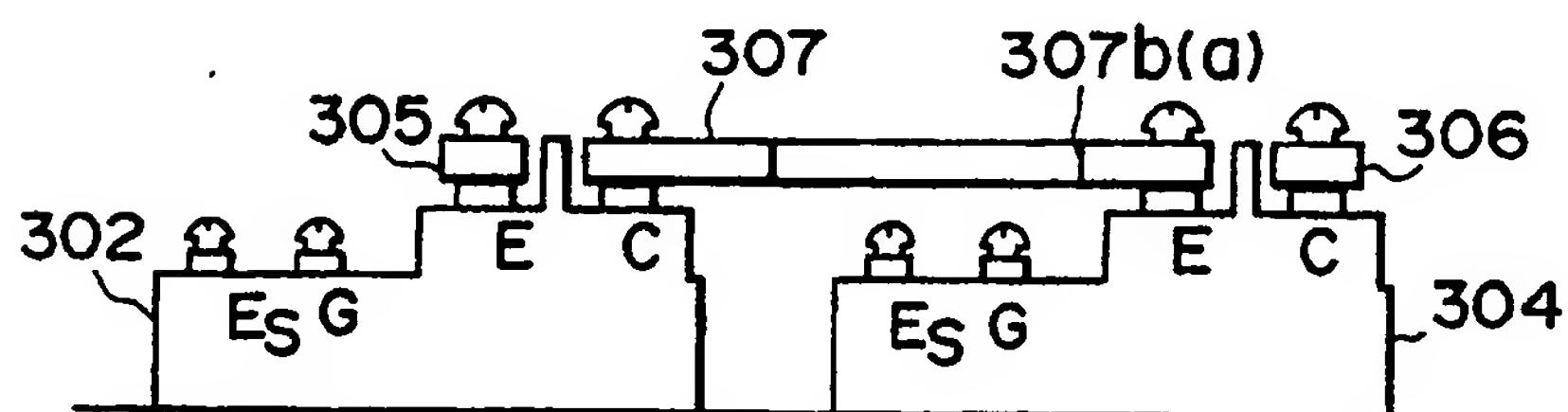


FIG. 2



F I G. 3A



F I G. 3B

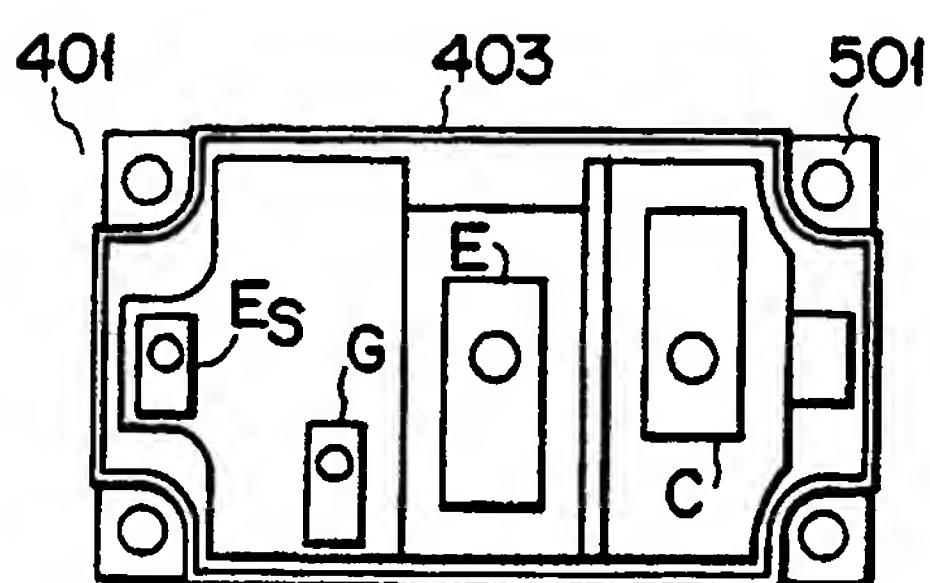


FIG. 4A

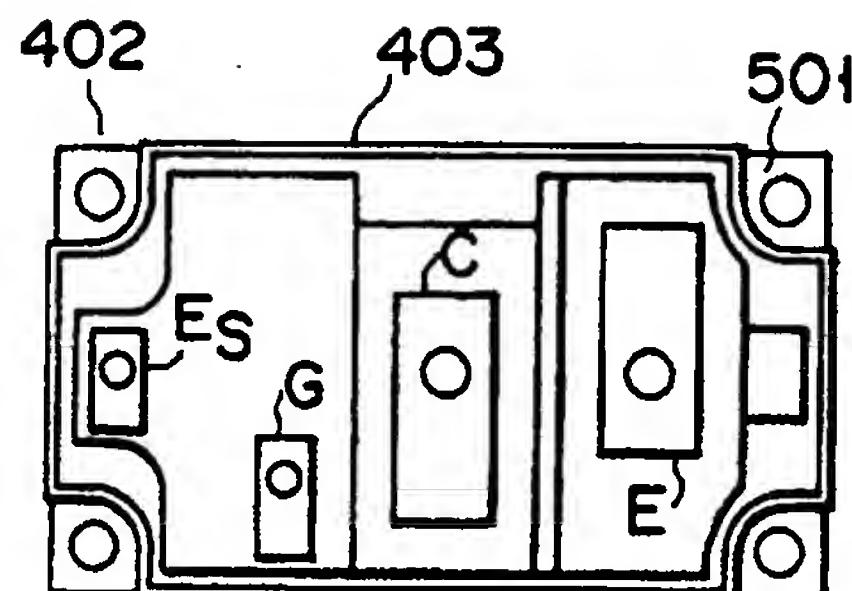


FIG. 4B

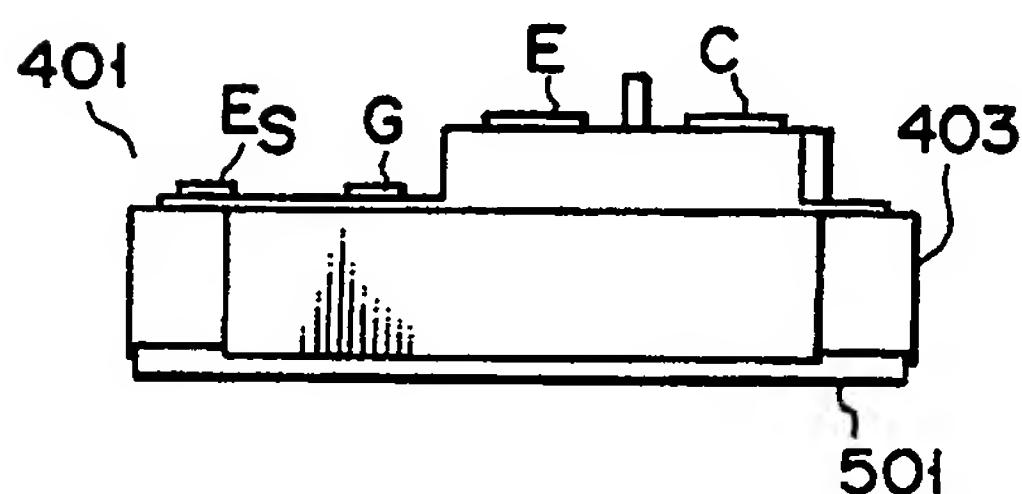


FIG. 4C

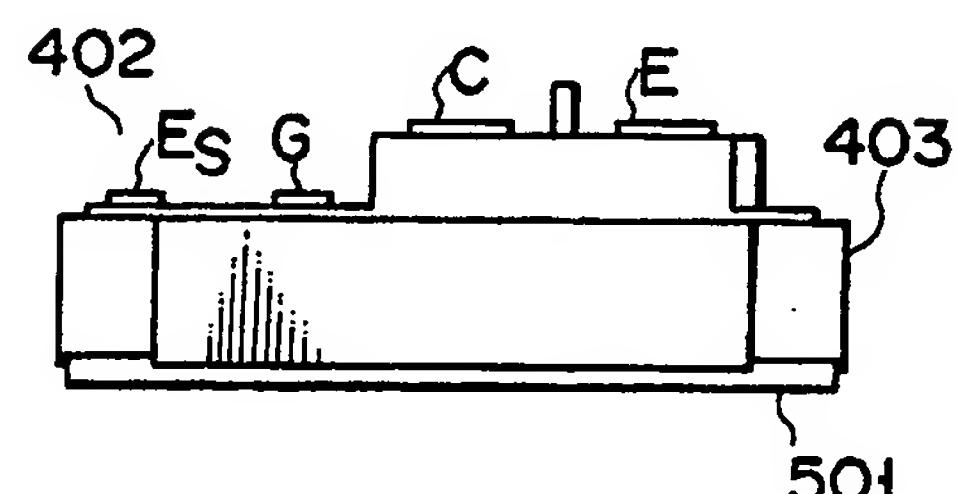


FIG. 4D

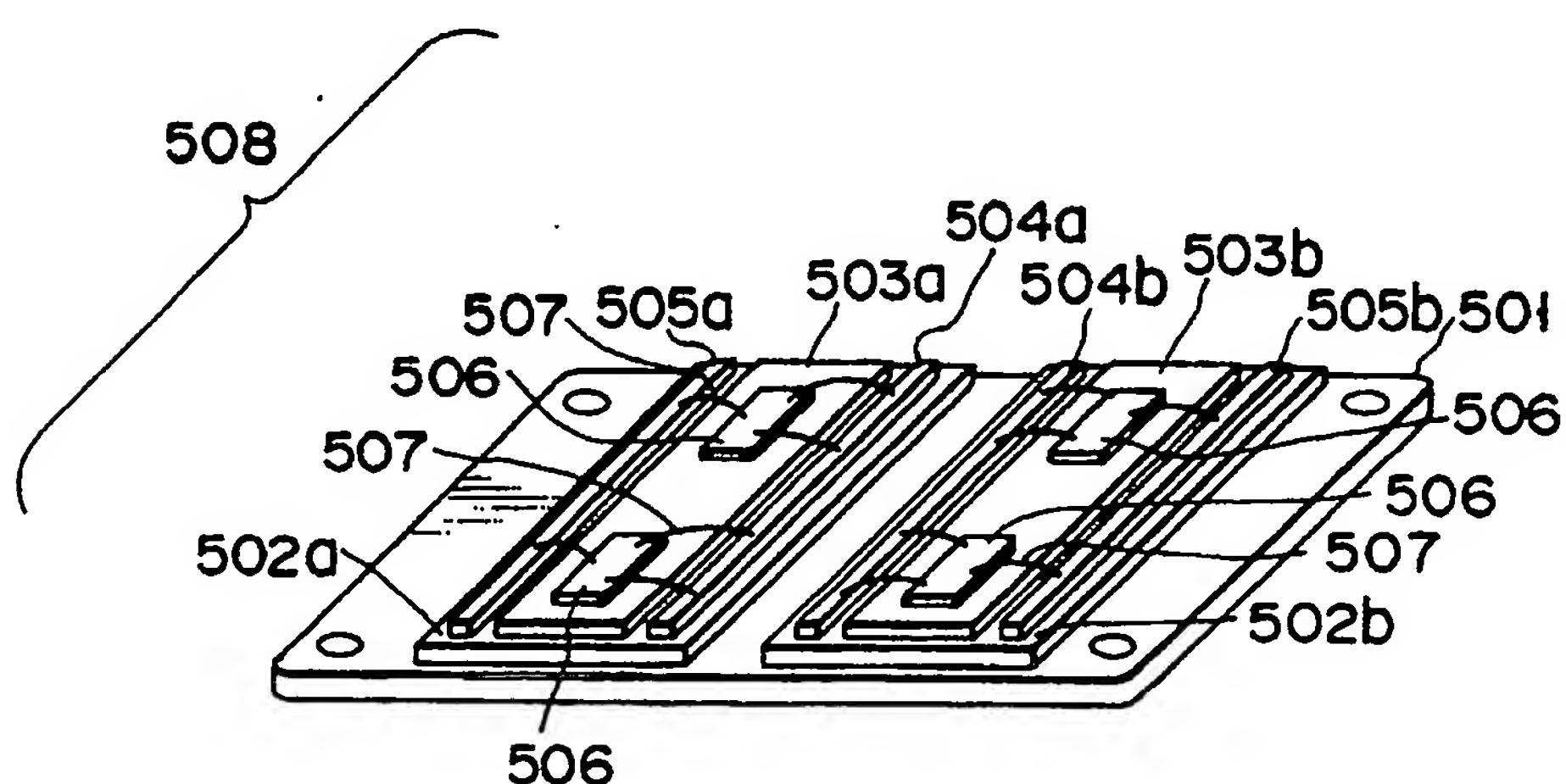
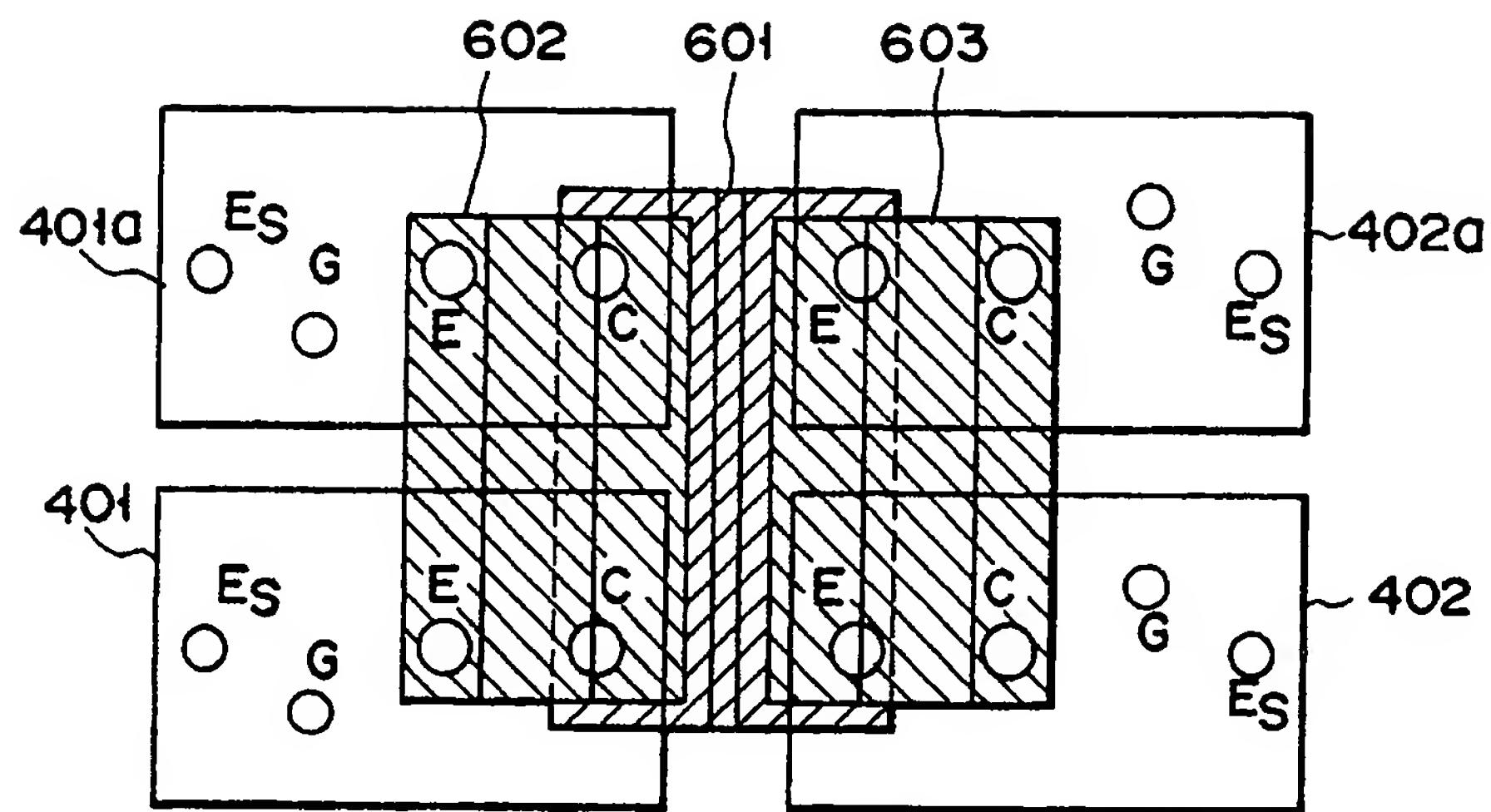
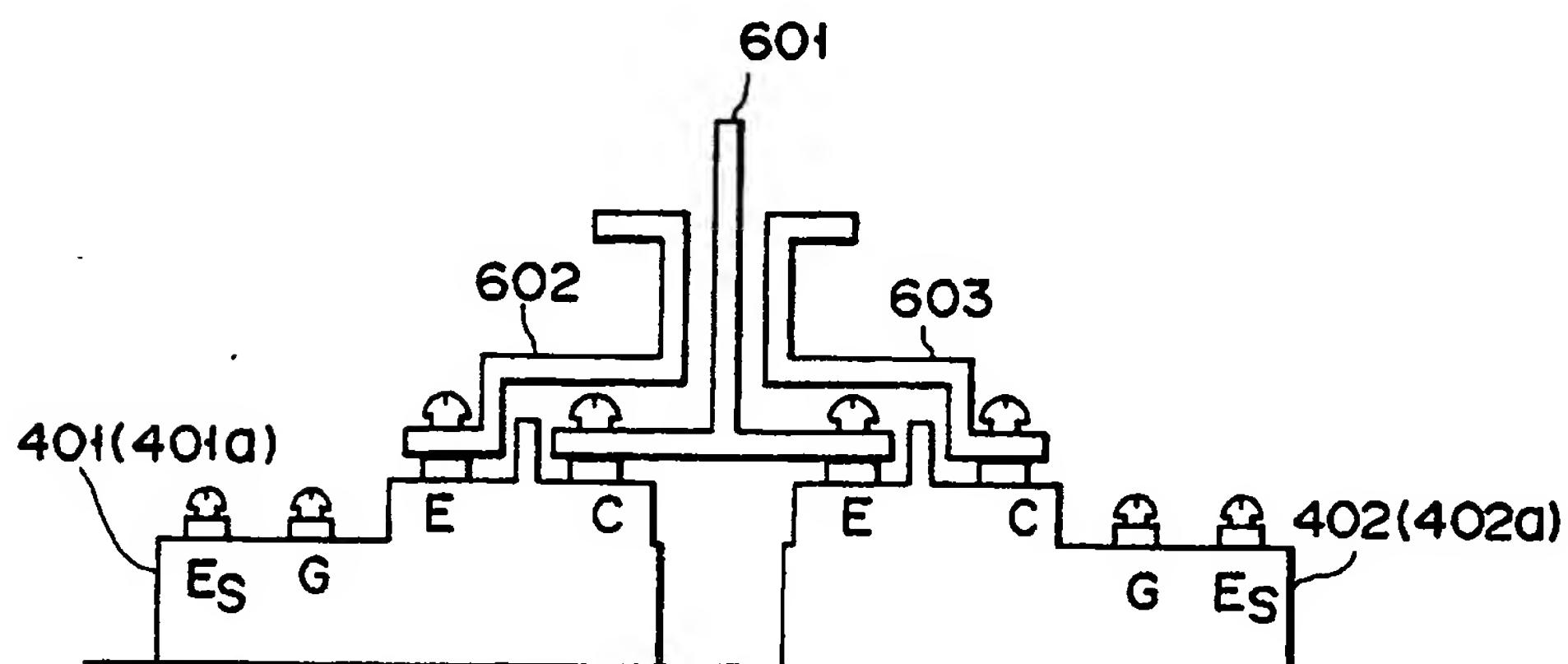


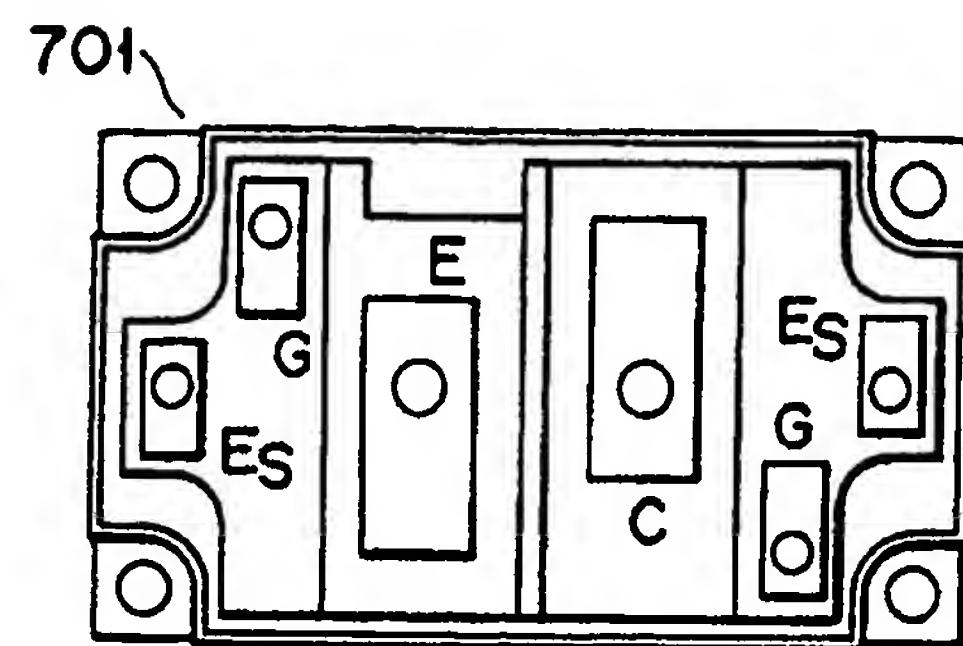
FIG. 5



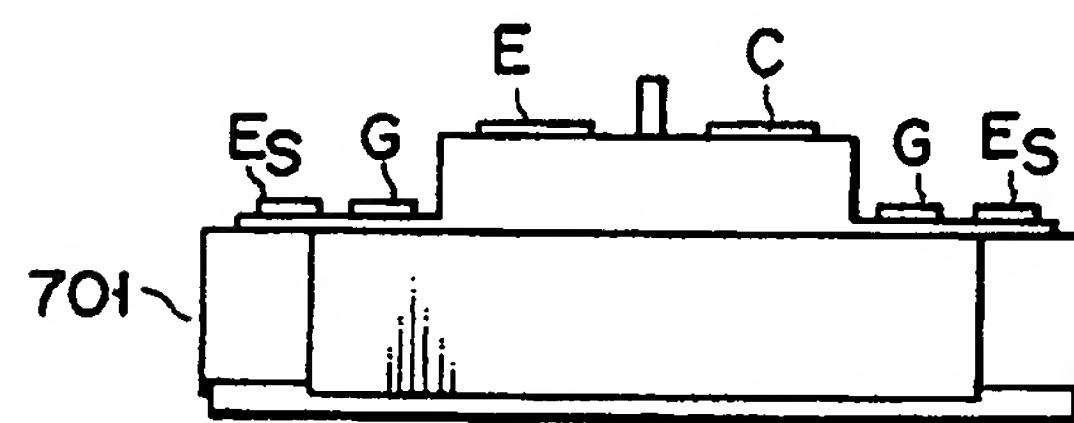
F I G. 6A



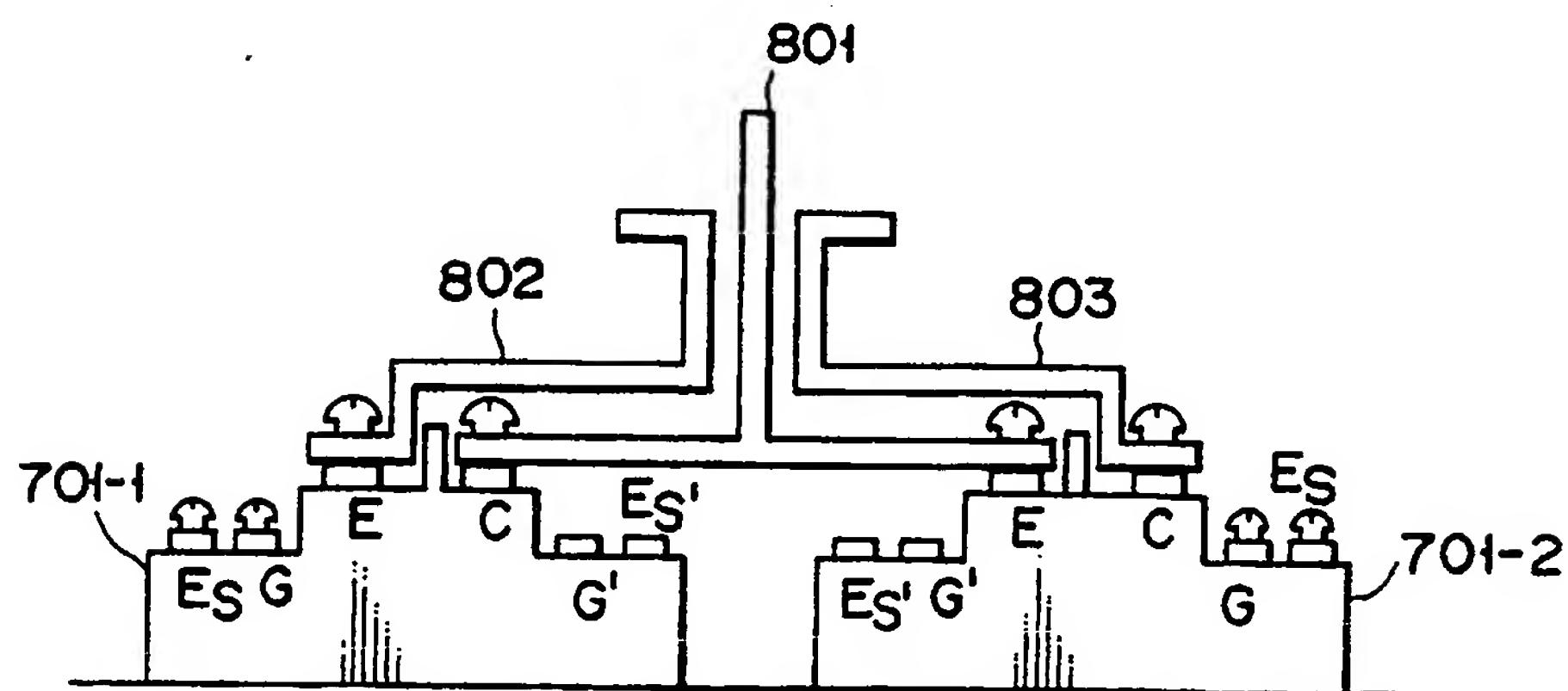
F I G. 6B



F I G. 7A



F I G. 7B



F I G. 8